REMARKS

Reconsideration and allowance of the subject application are respectfully requested. Claims 1-14 and 16-20 remain pending, claims 1, 9, and 14 being independent. In this amendment, Applicants have cancelled claim 15 and have amended claims 1, 8, 9, 13, 14, 16, and 20.

Rejection Under 35 U.S.C § 112, 2nd Paragraph

Claim 20 stands rejected under 35 U.S.C. 112, 2nd paragraph as allegedly being indefinite for failing to particularly point out distinctly claimed the subject matter that the Applicants regard as the invention. This rejection, insofar as it pertains to the presently pending claims, is respectively traversed.

As stated on page 2 of the Office Action, the outstanding rejection under 35 U.S.C. § 112, 2nd paragraph is based on the Examiner's conclusion that:

> [T]he method [of independent claim 14] is a method of using a joystick interface. Claim 20, however recites step for building the interface. Thus, it is not clear how this step is related to the above steps.

In response, Applicants have amended claim 20 in a manner that is believed to remove any inconsistency between claim 20 and independent claim 14.

In view of the above amendments to claim 20, Applicants respectfully request reconsideration and withdrawal of the outstanding rejection under 35 U.S.C. § 112, 2nd paragraph.

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Objection Under 37 CFR § 1.75

The Examiner has objected to claim 15 as allegedly being a substantial duplicate of claim 14. Applicants submit that the cancellation of claim 15 has rendered this objection moot and respectfully request reconsideration and withdrawal of the outstanding objection under 37 CFR § 1.75.

Prior Art Rejections

1. Rejection under 35 U.S.C. § 102

Claims 1-7, 9-12, and 14-19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by *Liu* (U.S. Patent 5,867,051). This rejection, insofar as it pertains to the presently pending claims, is respectfully traversed.

Independent claim 1 is directed to an interface between a joystick device having a first source voltage and a processor. As amended, the interface of claim 1 comprises: an RC network that is connected to the joystick device and includes a capacitor that generates an analog joystick position measurement signal; and an interface circuit having a second source voltage that is lower than the first source voltage (of the joystick device). The interface circuit of claim 1 includes: a buffer circuit that outputs a first logic state as a digital signal before the analog position measurement signal generated by the RC network capacitor exceeds a predetermined threshold and outputs a second logic state as the digital signal when the analog position measurement signal generated by the RC network capacitor exceeds the predetermined threshold;

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and a pulse generator that generates a pulse based on the digital signal output by the buffer circuit during a first mode of operation, the generated pulse having a width representing the coordinate position of the joystick device. As amended herein, claim 1 further recites that "the capacitance value of said capacitor [is] a function of said predetermined threshold that prevents deviation of the width of said pulse from expected values."

Thus, the device defined by claim 1 provides an interface between a joystick interface having a first source voltage, e.g., a standard 5 Volt joystick, using circuitry having a source voltage that is lower than the first source voltage, e.g., low-voltage CMOS integrated circuitry, to generate pulse widths representing joystick coordinate positions that conform to expected values. One exemplary application of this arrangement is to provide compatibility between a standard joystick device and various types of low-voltage integrated circuitry via proper selection of the RC network capacitor as a function of a buffer circuit threshold.

Liu discloses a digital joystick interface circuit that, as shown for example in Fig. 4, includes a game card 60 connected to a trigger detecting circuit 51 via a time delay that consists of a resistor R1 and a capacitor C1. The time delay generates a voltage that the trigger detecting circuit 51 compares to a reference voltage during joystick coordinate addressing. As discussed in column 1, *Liu* recognizes that variability in the voltage generated by the time delay circuitry of a conventional joystick interface may occur, for

example due to the effects of ambient temperature on the time delay capacitor. The interface circuit design disclosed by *Liu* seeks to compensate for such variability by providing a comparator circuit 54 that monitors the time required for a voltage generated by time delay circuitry to exceed a reference voltage relative to that of a joystick coordinate signal to achieve precise joystick coordinate addressing.

The joystick interface circuitry of *Liu* is not designed to provide compatibility between a joystick having a first source voltage, such as a standard 5 Volt joystick, and interface circuitry having a second source voltage that is lower than the first source voltage. Consequently, Applicants submit that *Liu* fails to anticipate an interface having the above-discussed features of claim 1. Applicants also submit that *Liu* fails to anticipate independent claims 9 and 14 based on similar reasoning.

Claims 2-7, 10-12, and 15-19, each depending either directly or directly from one of claims 1, 9, and 14, are not anticipated by *Liu* for at least the reasons set forth above, as well as on their own merits.

In view of the above, Applicants respectfully request reconsideration and withdrawal of the outstanding rejection of claims 1-7, 9-12, and 14-19 under 35 U.S.C. § 102 as being anticipated by *Liu*.

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2. Rejection under 35 U.S.C. § 103

Claims 8, 13, and 20 stand rejected under 35 U.S.C. §103 as being unpatentable over *Liu*. This rejection, insofar as it pertains to the presently pending claims, is respectfully traversed.

Claims 8, 13, and 20, depending directly from claims 1, 9, and 14 respectively, each recite a specific relationship between the capacitance value of the RC network capacitor and the predetermined threshold level used to generate the digital signal. In rejecting claims 8, 13, and 20 under 35 U.S.C. § 103 based solely on *Liu*, the Examiner states on page 4 of the Office Action that:

> In the Summary of the Invention, it is stated that one of the desired objective [sic] is the reduction of the voltage of the input signal. Thus, the selection of a capacitor for a voltage below the conventional 5 Volts is suggested.

Although less than clear, this reasoning seems to rely on the Applicants' own Summary of their invention as motivation for modifying the interface disclosed by *Liu*. This is clearly an improper basis for a rejection under 35 U.S.C. §103. *See e.g.*, MPEP § 2143 (stating that "[t]he teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure"). Further, this reasoning fails to address the specific feature recited in claims 8, 13, and 20, which does not merely refer to selecting a capacitor. Still further, it is not apparent from the stated grounds of rejection how the interface circuitry of *Liu* is being

modified to allegedly satisfy the features of these claims. In short, the stated grounds of rejection fails to establish *prima facie* obviousness of dependent claims 8, 13, and 20.

In view of the above, Applicants respectfully request reconsideration and withdrawal of the outstanding rejection of claims 8, 13, and 20 under 35 U.S.C. § 103 as being unpatentable over *Liu*.

Conclusion

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact D. Richard Anderson (Reg. No.40,439) at (703) 205-8000, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicant(s) respectfully petition(s) for a two (2) month extension of time for filing a reply in connection with the present application, and authorizes the Commissioner to charge Deposit Account No. 12-2325 in the amount of $390.00.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 12-2325 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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